TIME-MULTIPLEXING DATA BETWEEN ASYNCHRONOUS CLOCK DOMAINS WITHIN CYCLE SIMULATION AND EMULATION ENVIRONMENTS

Abstract of the Disclosure

An apparatus and method utilize a buffer interposed in a common signal path between asynchronous clock domains in a hardware-based logic emulation environment to manage the communication of time-multiplexed data signals between the clock domains during hardware-based emulation. The buffer is effectively used to latch each data signal communicated across the common signal path so that the clock domain that receives the signals can retrieve each such signal at appropriate points in the receiver clock domain's evaluation cycle. Independently-controlled write/read pointers are maintained in a buffer control circuit to independently address the buffer for the transmitter and receiver sides of an asynchronous communication path. Locations in the buffer are associated with specific steps in the evaluation cycles of each of the transmitter and receiver clock domains, and the write/read pointers are managed to respectively write and read data to and from the locations in the buffer based upon the current evaluation steps being performed within the respective evaluation cycles of the transmitter and receiver clock domains.